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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/700,359	11/14/2000	Roger Green Stewart	RCA89038	4790

7590 09/09/2003

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EXAMINER
NELSON, ALECIA DIANE

ART UNIT	PAPER NUMBER
2675	12

DATE MAILED: 09/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/700,359	STEWART ET AL.	
	Examiner	Art Unit	
	Alecia D Nelson	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. ***Claims 1-6*** are rejected under 35 U.S.C. 102(b) as being anticipated by Shinya (U.S. Patent No. 5,170,158).

Shinya teaches an arrangement for transferring pixel information with respect to pixels arranged in columns and rows of an array of a display device (see abstract). The display device comprises a plurality of semiconductor switches, each having a first, second, and third terminal (see S/H), a control bus (see wires (SCK1-5)) coupled to a the terminals of each of the plurality of switches (right input terminal of S/H) for communicating corresponding signals, and a plurality of local buses (wires in groups of five from left input of the sample hold circuit to the DAC) that are separated from one another for communicating corresponding signals, a given local bus having a first bus section coupled to a second plurality of terminals associated with the given local bus (portion extending from DAC) and extending in a manner to cross over the control bus (over SCK1-5) and a second bus section extending from the first bust section and having conductors thereof coupled in a local, clustering bus arrangement (portion after crossing SCK1-5 ending in the left input of the sample hold circuits) to the second

terminals of switches associated with the given local bus of the plurality of switches, the associated switches having the third terminals thereof coupled to consecutively disposed column conductors (0_0-0_{99}), respectively of the array (see figure 18). With reference to **claim 2**, it is also taught a timing generator (14) providing switch control signals and DACs providing picture information signals to the S/H. Since each of the 20 outputs of the DACs is coupled to five sample hold circuits, a 1 of 5 demultiplexing is achieved under the control of the timing generator (14) (see column 9, line49-column 10, line19). With reference to **claim 3**, there is also disclosed that each of the sub groups is coupled to the same wire SCK of the timing generator (14) (see figure 18). With further reference to **claim 4**, Shinya teaches in figure 18 that the conductors of the second bus section of the given local bus are disposed in a vicinity of the switches associated with the given bus and remotely from switches associated with the other local buses of the plurality of local buses to provide bus separation for obtaining the local clustering bus arrangement (see figure 18). Referring to **claim 5**, it can be seen that the conductors of the first bus (SCK1-5) extend along the plurality of semiconductor switches. With reference to **claim 6**, it is further taught that the data line drivers are controlled by the wire (OE) from the timing generator.

3. ***Claims 7-9*** are rejected under 35 U.S.C. 102(b) as being anticipated by Inoue et al. (U.S. Patent No. 5,113,181).

With reference to the claims Inoue et al. teaches in figure 2 a n x m matrix wiring

circuit connected to M signal lines (m<M) for the N x M active matrix (see col. 4, lines 2-8) for a display panel comprising a plurality of clusters of switches (6), each cluster having numbered switches 1 thru n arranged sequentially, and each switch (6) having respective input, output, and control terminals (see column 3, line 61) with control terminals of all switches in each cluster connected to a common control terminal (see col. 3, line 63-col. 4, line 12), and having respective output terminals coupled to successive data lines (S(1)-S(n)) on the display panel, a plurality of groups of data buses, each group of data buses having numbered conductors 1 thru n, the numbered conductors of respective groups of data buses being coupled to input terminals of corresponding numbered switches (6) of a plurality of certain groups of switches (block 1-4), a control bus including a plurality of conductors, the control bus arranged to crossover the plurality of clusters of data buses (see column 3, lines 24-26, column 5, lines 30-37), and connections between one of the plurality of conductors of the control bus and respective common control terminals of the groups of switches (see figure 2).

Response to Arguments

4. Applicant's arguments filed 01/03/03 have been fully considered but they are not persuasive. With reference to **claims 1-6**, the applicant argues that Shinya neither discloses nor suggest a plurality of local buses that are separated from one another having a first bus section extending in a manner to cross the control bus. However, Shinya clearly teaches a plurality of local buses extending from DAC, that are separated from one another, having a first bus section extending in a manner to cross the control

buss (SCK1-5). Further it is stated that Shinya neither discloses or suggest a plurality of local buses that are separated from one another. However, the conductors, representing the local bus, extend from DAC separately. The conductor then goes into the different S/H. Therefore it is clear that the conductors representing the local buses are separated from one another. Further it is stated how the conductors of the control bus and the local bus cross each other in order to minimize the number of crossovers. However, it is not claimed that the control bus only crosses the local bus once or a minimal amount of times. With reference to **claims 7-9**, the applicant argues that Inoue et al. fails to disclose or suggest that a plurality of groups of data buses, each group having numbered conductors. However it can be seen in Figure 2, a group of data buses extending from each of blocks 1-4. Further it is argued that Inoue et al. neither discloses or suggest that the numbered conductors of respective groups of data buses are coupled to input terminals of corresponding numbered switches of a certain switch group within a plurality of switch groups. However each of the data buses extending from each of the blocks 1-4 are connected to a terminal of a plurality of switches (6) corresponding to each of the conductors extending from the blocks. Further it is argued that Inoue et al. disclose each image signal line being coupled to an input terminal of a switch in every switch group. However, it is claimed that the numbered conductors of the groups of data buses is coupled to input terminals of corresponding numbered switches of a certain switch group (block 1) of a plurality of switch groups (blocks 1-4). It is also argued that Inoue et al. fails to teach a control bus including a plurality of conductors being arranged to cross a plurality of groups of data buses. However, it

then stated by the applicant that, Inoue et al. includes a plurality of conductive lines and a plurality of switching signal lines crossing the conductive lines. Therefore it is taught a control bus extending horizontally to cross the plurality of data buses.

Accordingly, the rejection to **claims 1-7** will be maintained.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703)305-0143. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras can be reached on (703)305-9720.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-2600.

And/ADN
September 4, 2003

DENNIS-DOON CHOW
PRIMARY EXAMINER